REMARKS

Claims 1 through 39 and 44 through 53 are currently pending in the application.

Claims 40, 41, 42, 43, 54, and 55 have been canceled.

Claims 1 through 31 are withdrawn from consideration as being directed to a non-elected invention.

Claims 32 through 55 currently stand rejected.

This amendment is in response to the Office Action of September 18, 2001.

Applicants hereby affirm the election to prosecute claims 32 through 55.

Applicants submit herewith, under cover of a separate Submission of Proposed Drawing Amendment, for proposed corrections to FIGS. 5, 7, and 8 of the drawings. All proposed corrections have been marked in red. Applicants respectfully request approval of the corrections to the drawings and will file corrected formal drawings upon receipt of such approval and a Notice of Allowance and Issue Fee Due in the application. Previously, in a Preliminary Amendment filed on December 12, 2000, FIG. 9 of the drawings was corrected for approval by changing the numeral "30B" to–30C–. In the Office Action, no mention was made regarding the approval of such drawing correction.

Claims 35 through 37 and 47 through 49 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Accordingly, Applicants have amended the specification at 6, line 21, after the word "a", inserting the words —flowable, hardenable, polymeric— to describe the glob-top material. As the claims of the originally application are part of the disclosure thereof, Applicants have complied with 35 U.S.C. § 132 as no new matter has been added to the application by such an amendment.

Claims 32 through 55 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Accordingly, Applicants have amended claims 32 and 44 to

delete the language "configured for opposite side access between attached semiconductor dice . . . and the plurality of bond pads". Therefore, claims 32 through 55 clearly comply with the provisions of 35 U.S.C. § 112, second paragraph.

Claim 43 was objected to under 37 C.F.R. § 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Claim 43 has been canceled.

Claims 32 through 37, 39, 40, 44 through 49, 51 and 52 were rejected under 35 U.S.C. § 102(e) as being anticipated by Chan et al.

Claims 32, 38, 40, 44, 50 and 52 were rejected under 35 U.S.C. § 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Chiu.

Claims 35 through 37, 39, 47 through 49 and 51 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiu in view of Chan et al.

Claims 41 and 53 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiu in view of Swamy et al.

Claims 42, 54 and 55 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiu in view of Swamy et al. and the admitted prior art.

Claims 41 and 53 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chan et al. in view of Akram.

Claims 42, 54 and 55 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chan et al. in view of Akram and Swamy and the admitted prior art.

Applicants have amended the claimed invention as suggested by the Examiner for the presently claimed invention to particularly point out and distinctly claim the subject matter of the invention to comply with the provisions of 35 U.S.C. § 112. Therefore, presently amended claims 32 through 39 and 44 through 53 are allowable under the provisions of 35 U.S.C. § 112.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited prior art.

Applicants submit that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants further submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Applicants submit that presently amended independent claims 32 and 44 are clearly allowable over the Chan et al. reference or the Chiu reference under 35 U.S.C. § 102 because neither Chan et al. reference nor the Chiu reference identically describes, either explicitly or inherently, each and every element of the claimed invention in the same detail as set forth in either presently amended independent claim 32 or 44. For instance, neither the Chan et al. reference nor the Chiu reference, at the very least, contains the element of the presently claimed invention of amended independent claims 32 and 44 calling for "said forming an input/output connector comprising forming a ball-grid-array on one of said first and second sides of said substrate in a peripheral area surrounding said dice". Applicants submit that neither the Chan et al. reference nor the Chiu reference contains any such element whatsoever.

Therefore, claims 32 through 39 and 44 through 53 are allowable.

Turning to the presently amended independent claims 32 and 44 regarding any rejection thereof based upon the Chiu reference under 35 U.S.C. § 103, Applicant submit that the Chiu reference does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding

the presently claimed invention of amended independent claims 32 and 44 because, at the very least, the Chiu reference contains no suggestion therein for any modification thereof, the Chiu reference does not teach or suggest all the limitations of the presently claimed invention, and any rejection of the presently claimed invention would be a hindsight reconstruction of the presently claimed invention based solely upon Applicants' disclosure, not the cited prior art. For instance, Applicants submit that the Chiu reference does not teach or suggest the claim limitation of the presently claimed invention of amended independent claims 32 and 44 calling for "said forming an input/output connector comprising forming a ball-grid-array on one of said first and second sides of said substrate in a peripheral area surrounding said dice". The Chiu reference contains no such disclosure whatsoever. Accordingly, the Chiu reference cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103.

Additionally, any rejection of the presently claimed invention would be a hindsight reconstruction of the claimed invention based solely upon Applicants' disclosure, not the cited prior art since the cited prior art does not teach or suggest all the limitations of the presently claimed invention. Such a rejection is neither within the ambit nor purview of 35 U.S.C. § 103 and, clearly, improper.

Therefore, presently amended independent claims 32 and 44 are allowable as well as presently pending claims 33 through 39 and 45 through 53 therefrom.

Turning to any rejection of presently amended independent claims 32 and 44 based upon either the Chan et al. reference or the Chiu reference either in view of the Swamy et al. reference, the admitted prior art, and/or the Akram reference, Applicants submit that any rejection of the presently claimed invention of amended independent claims 32 and 44 based solely or upon any combination of the cited prior art under 35 U.S.C. § 103 fails to establish a *prima facie* case of obviousness because there is no suggestion for any modification of either the Chan et al. reference or the Chiu reference, there is no teaching or suggestion in the cited prior art for the present limitations of the claimed invention, and any rejection of the presently claimed invention would be a hindsight reconstruction of the claimed invention based solely upon

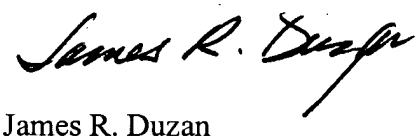
Applicants' disclosure, not the cited prior art. At the very least, any proposed combination of the cited prior art fails to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 because the claim limitation calling for "said forming an input/output connector comprising forming a ball-grid-array on one of said first and second sides of said substrate in a peripheral area surrounding said dice" is not taught or suggested in any of the cited prior art.

Additionally, any rejection of the presently claimed invention would be a hindsight reconstruction of the claimed invention based solely upon Applicants' disclosure, not the cited prior art since the cited prior art does not teach or suggest all the limitations of the presently claimed invention. Such a rejection is neither within the ambit nor purview of 35 U.S.C. § 103 and, clearly, improper.

Therefore, claims 32 through 39 and 44 through 53 are allowable.

Applicants request the allowance of claims 32 through 39 and 44 through 53 and the case passed for issue.

Respectfully submitted,



James R. Duzan
Attorney for Applicants
Registration No. 28,393
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110
(801) 532-1922

Date: December 18, 2001
JRD/sls:jml

Enclosure: Appendix A – Version with Markings to Show Changes Made

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APPENDIX A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

A marked-up version of the amended paragraphs in the specification, highlighting the changes thereto, follows to clearly identify the amendments:

Please replace the sixth full paragraph on page 6 with the following:

Each of the IC dies 12A, 12B and 14A is a bare (unpackaged) die with one or more adjacent rows of bond pads 22 on an active side 24. In drawing FIGS. 1 and 2, the bond pads 22 of dies on the opposite side are not visible, being covered by a flowable, hardenable, polymeric glob-top 40. In drawing FIGS. 5 to 8, two rows of bond pads 22 are shown spanning the minor dimension 26 of the dies (See FIG. 1). Alternatively, the bond pads 22 may be configured in a row or rows anywhere on the active surface 24, but preferably along a centerline 42 of a major dimension 28 or minor dimension 26, or even at an oblique angle with the major dimension. Preferably, the dice 12, 14 should be aligned so that the rows of bond pads 22 are in a parallel, spaced apart relationship.

Please replace the sixth full paragraph on page 9 with the following:

Conductive patterns 34A, 34B are formed on sides 16,18, respectively, of the substrate 20, such as by a lithographic metallization process or by other methods known in the art. The conductive patterns 34A, 34B include conductors [35] 35A having one end configured as a wire-connecting site 32 adjacent a through-slot 30, and the other end is configured for attachment to an input/output connection. Where the through-slot 30 is stepped, the wire-connecting sites 32 are positioned on the stepped surfaces 58.

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

32. (Two Times Amended) A method for forming a high density multi-chip module, comprising [the steps of]:

providing a plurality of integrated circuit semiconductor dice, each semiconductor die of said plurality having an active surface having a plurality of bond pads thereon;

forming a substrate with opposing first and second sides, at least three elongate through-slots extending from said first side to said second side[, each of said at least three through-slots configured for opposite side access between attached semiconductor dice of said plurality of semiconductor dice and the plurality of bond pads of a semiconductor die of said plurality of semiconductor dice bonded to said substrate];

forming a pattern of a plurality of electrical conductors associated with said substrate one each said first side and second side of said substrate, at least one electrical conductor of said plurality of electrical conductors having a connection terminal adjacent a through-slot of said at least three through-slots for connecting said plurality of bond pads of a semiconductor die of said plurality of semiconductor dice to an input/output connector;

connecting said conductor pattern on said first side and said second side of said substrate with conductive vias through said substrate;

forming an input/output connector on said substrate and connecting said input/output connector to said plurality of electrical conductors, said forming an input/output connector comprising forming a ball-grid-array on one of said first and second sides of said substrate in a peripheral area surrounding said plurality of semiconductor dice;

attaching the active surfaces of a plurality of said plurality of semiconductor dice to the first side of said substrate wherein the bond pads thereof are aligned with alternate through-slots of said at least three through-slots for access from the second side of said substrate;

attaching the active surface of at least one semiconductor die of said plurality of semiconductor dice to said second side of said substrate, the plurality of bond pads of said at least one semiconductor die aligned with other alternate through-slots of said at least three through-slots for access from the first side of said substrate; and

wire-bonding said plurality of bond pads of each attached semiconductor die of said plurality of semiconductor dice to connection terminals adjacent the alternate through-slots.

34. (Two Times Amended) The method of claim 33, wherein [the step of] forming a pattern of electrical conductors includes forming conductive connection terminals on said elongate stepped surface.

35. (Two Times Amended) The method of claim 32, further comprising [the step of]: inserting a flowable hardenable glob-top material into each said through-slot to encapsulate wires therein.

38. (Amended) The method of claim 32, further comprising [the step of]: performing electrical testing of said plurality of semiconductor dice following wire-bonding thereof and prior to wire encapsulation.

39. (Two Times Amended) The method of claim 32, further comprising [the step of]: encapsulating said plurality of dice with a polymeric sealant.

44. (Two Times Amended) A method for forming a high density multi-chip module, comprising [the steps of]:

providing a plurality of integrated circuit dice, each die of said plurality having an active surface with a row of conductive bond pads thereon;

forming a planar substrate with opposing first and second sides, at least three elongate through-slots extending from said first side to said second side[, each of said at least three through-slots configured for opposite side access between attached dies of said plurality of dice and the conductive bond pads of a die of said plurality bonded to said substrate];

forming a pattern of electrical conductors associated with said substrate and having connection terminals adjacent each of said at least three through-slots for connecting said bond pads to an input/output connector;

forming an input/output connector on said substrate and connecting said input/output connector to said electrical conductors from said bond pads, said forming an input/output connector comprising forming a ball-grid-array on one of said first and second sides of said substrate in a peripheral area surrounding said dice;

attaching the active surfaces of a plurality of said plurality of integrated circuit dice to said first side of said substrate wherein the bond pads thereof are aligned with alternate through-slots of said at least three through-slots for access from the second side of said substrate;

attaching the active surface of at least one of said plurality of dice to said second side of said substrate wherein the bond pads thereof are aligned with other alternate through-slots for access from the first side of said substrate; and

wire-bonding said bond pads of each attached die to connection terminals adjacent the corresponding through-slot.

46. (Two Times Amended) The method of claim 45, wherein [the step of] forming a pattern of electrical conductors includes forming conductive connection terminals on said stepped surface.

47. (Two Times Amended) The method of claim 44, further comprising [the step of] inserting a flowable hardenable glob-top material into each said through-slot to encapsulate wires therein.

50. (Amended) The method of claim 44, further comprising [the step of]: performing electrical testing of said dice following wire-bonding thereof and prior to wire encapsulation.

51. (Two Times Amended) The method of claim 44, further comprising [the step of]: encapsulating said dice with a polymeric sealant.

52. (Two Times Amended) The method of claim 44, wherein [the step of] forming a pattern of electrical conductors on said substrate comprises forming a conductor pattern on each of said first and second sides of said substrate.

53. (Amended) The method of claim 52, further comprising [the step of]: connecting said two conductor patterns with conductive vias through said substrate.